In the Claims:

1.-32. (Canceled)

33. (Original) A multi-layer semiconductor wafer structure defining a multiplicity of dies formed thereon, said wafer structure comprising:

a first scribe line having a selected width extending along a first direction;

a second scribe line having a selected width extending along a second direction and intersecting said first scribe line;

four dies located at and separated by the intersection of said first and second scribe lines wherein each of the four dies comprises a corner point adjacent the intersection of said first and second scribe lines;

a first free area A_1 on the first scribe line adjacent the corner point of the first die, wherein A_1 is defined by the equation $A_1=D_1xS_1$ and wherein D_1 is the distance extending from the corner point of the first die, and S_1 is the width of the first scribe line;

a second free area A_2 on the second scribe line adjacent the corner point of the second die, wherein A_2 is defined by the equation $A_2=D_2xS_2$, and wherein D_2 is the distance from the corner point of the second die, and S_2 is the width of the second scribe line;

a third free area A_3 on the second scribe line adjacent the third corner point of the third die, wherein A_3 is defined by the equation $A_3=D_3xS_2$, and wherein D_3 is the distance from the corner point of the third die;

a fourth free area A_4 on the first scribe line adjacent the corner point of the fourth die, wherein A_4 is defined by the equation $A_4=D_4xS_1$, and wherein D_4 is the distance from the corner point of the fourth die; and

a fifth free area A_S on the intersection of the first scribe line and the second scribe line and is defined by the equation $A_S=S_1xS_2$.

34. (Original) The semiconductor wafer of claim 33 further comprising:

at least one test key formed on at least one of the free areas A_1, A_2, A_3, A_4 and A_S;

wherein a first measurement ratio R_1 is defined as the equation $R_1=M_1/A_1$, wherein M_1 is the total area of the test keys formed on the first free area A_1;

wherein a second measurement ratio R_2 is defined as the equation: $R_2= M_2/A_2$, wherein M_2 is the total area of the test keys formed on the second free area A_2;

wherein a third measurement ratio R_3 is defined as the equation: $R_3= M_3/A_3$, wherein M_3 is the total area of the test keys formed on the third free area A_3;

wherein a fourth measurement ratio R_4 is defined as the equation: $R_4= M_4/A_4$, wherein M_4 is the total area of the test keys formed on the fourth free area A_4;

wherein a fifth measurement ratio R_S is defined as the equation: $R_S= M_S/A_S$, wherein M_S is the total area of the test keys formed on the fifth free area A_S; and

wherein a total measurement ration R is defined as the equation $R=(M_1+M_2+M_3+M_4+M_S) / (A_1+A_2+A_3+A_4+A_S)$.

35. (Original) The semiconductor wafer of claim 34 wherein the first measurement ratio R_1 is less than about 10%.

36. (Original) The semiconductor wafer of claim 33 wherein the distance D_4 is less than about 600μm.

37. (Original) The semiconductor wafer of claim 33 wherein the width S_1 of the first scribe line is greater than about 20μm.

38. (Original) The semiconductor wafer of claim 33 wherein the width S_2 of the second scribe line is greater than about 20μm.

39. (Original) The semiconductor wafer of claim 33 wherein the multi-layer structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs and InP.

40. (Original) The semiconductor wafer of claim 33 wherein each of said four dies comprises:

a first peripheral region parallel to said first scribe line;

a second peripheral region parallel to said second scribe line;

a conductive ring formed between said die and said first peripheral region and said second peripheral region; and

an array of apertures formed in the conductive ring and adjacent the corner area of the die.

41. (Previously Presented) The semiconductor wafer of claim 33 wherein at least one layer of the multilayered wafer structure is a low-k dielectric layer having a dielectric constant less than approximately 3.5.

42. (Original) The semiconductor wafer of claim 40 wherein the array of apertures comprises two rows of holes.

43. (Original) The semiconductor wafer of claim 41 wherein said array of apertures comprises at least two slots.

44. (Original) The semiconductor wafer of claim 40 wherein the array of apertures extends along at least one of the first peripheral region and the second peripheral region.

45. (Original) The semiconductor wafer of claim 40, wherein each of the four dies further comprises a circuit area with a plurality of circuit elements, wherein the conductive ring is electrically connected to the circuit elements to apply one of a power source and a ground potential to the circuit elements.

46. (Original) The semiconductor wafer of claim 40 wherein the conductive ring has a width of between about 50μm and 300μm.

47.-65. (Canceled)